IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An image processing circuit processing raw image data picked up with an image pickup device, comprising:

means for A/D converting said raw image data, wherein said raw image data is image data to which no pixel interpolation has been performed;

means for compressing the raw image data converted by and transferred from said A/D converting means;

means for temporarily storing compressed data transferred from said compression means;

means for reading said compressed data from said means for temporarily storing compressed data and expanding the same; and

means for executing image processing on expanded data transferred from said expansion means.

Claim 2 (Previously Presented): The image processing circuit according to claim 1, wherein said image pickup device is driven by an interlacing system reading an odd field consisting of only odd lines and an even field consisting of only even lines forming a frame at temporally different timings,

said means for temporarily storing compressed data stores said compressed data of a first field formed by either said odd field or said even field, and

said means for executing image processing reads said first field stored in said means for temporarily storing compressed data in synchronization with entry of a second field formed by remaining said field and executes real-time image processing on said first and second fields.

Claim 3 (Previously Presented): The image processing circuit according to claim 1 or 2, wherein

data transfer between said compression means and said means for temporarily storing compressed data, and data transfer between said means for expanding and said means for temporarily storing compressed data are controlled by a direct memory access system.

Claim 4 (Previously Presented): The image processing circuit according to claim 1, further comprising:

means for dividing said raw image data into a plurality of blocks and outputting the same to said means for compressing, wherein

said means for compressing and said means for expanding execute compression and expansion in units of said blocks.

Claim 5 (Previously Presented): The image processing circuit according to claim 4, further comprising:

means for detecting a block including previously specified defective pixel data among said expanded data expanded by said means for expanding and outputting a block obtained by correcting said defective pixel data to said means for compressing.

Claim 6 (Previously Presented): The image processing circuit according to claim 4, further comprising:

means for performing a defect inspection before outputting said expanded data expanded by said means for expanding to said means for executing image processing for

replacing a block having detected defective pixel data with a normal block and outputting the same to said means for compressing.

Claim 7 (Currently Amended): The image processing circuit according to any of claims 4 to 6, wherein

said means for dividing divides said ~~digital~~ raw image data into a plurality of blocks in units of lines.

Claim 8 (Previously Presented): The image processing circuit according to claim 1 or 2, further comprising:

means for calculating the difference between pixel values of said raw image data and outputting said difference to said means for compressing before compressing said raw image data in said compression means.

Claim 9 (Previously Presented): The image processing circuit according to claim 8, wherein

said means for calculating calculates the difference between the values of pixels adjacent to each other along a time base.

Claim 10 (Previously Presented): The image processing circuit according to claim 8, wherein

said means for calculating calculates the difference between the values of alternate pixels along a time base.

Claim 11 (Previously Presented): The image processing circuit according to claim 8, wherein

said means for calculating calculates the difference between the values of vertically adjacent two pixels of two lines of said raw image data.

Claim 12 (Previously Presented): The image processing circuit according to claim 8, wherein

said means for calculating calculates the difference between the values of vertically adjacent two pixels of alternate lines of said raw image data.

Claim 13 (Previously Presented): The image processing circuit according to claim 8, wherein

said means for calculating, which calculates the difference between the values of vertically adjacent two pixels of alternate lines or two lines of said raw image data, is selected in response to a driving system for said image pickup device.

Claim 14 (Currently Amended): A method for processing raw image data picked up with an image pickup device, comprising the steps of:

A/D converting said raw image data, wherein said raw image data is image data to which no pixel interpolation has been performed;

compressing the raw image data converted in said A/D converting step;

temporarily storing compressed data compressed in said compression step;

reading said compressed data from storage;

expanding said compressed data read from storage; and

executing image processing on expanded data expanded in said expanding step.

Claim 15 (Currently Amended): An image processing apparatus for processing raw image data picked up with an image pickup device, comprising:

an A/D converter configured to A/D convert said raw image data, wherein said raw image data is image data to which no pixel interpolation has been performed;

a compressor configured to compress the raw image data converted by and transferred from said A/D converter;

a buffer configured to temporarily store compressed data transferred from said compressor;

an expander configured to read said compressed data from said buffer and expanding the same; and

an image processor configured to execute image processing on expanded data transferred from said expander.